

IN THE CLAIMS:

Please amend claims 1-5 and 12 as follows:

*Sub  
D/b22*

1. (Twice Amended) An information processing system comprising:  
a processor;  
a memory;  
a memory controller;  
a system bus connecting said processor and said memory controller;  
and;  
at least two memory buses connecting said memory controller and said  
memory, said at least two memory buses comprising:  
a first memory bus for transferring an instruction code, and  
a second memory bus for transferring data,  
said memory controller comprising:  
a buffer,  
a control circuit, and  
an access judging circuit, wherein;  
said control circuit estimates a most probable address to be  
accessed next in said memory, and  
said access judging circuit prefetches data stored in said most  
probable address of the memory into the buffer.

B22  
2. (Twice Amended) An information processing system according to claim 1, wherein said memory controller comprises a direct path for transmitting data directly to said processor from said memory therethrough.

3. (Twice Amended) An information processing system according to claim 1, wherein said memory stores said instruction code to be executed on said processor therein, and said control circuit prefetches the instruction code into said buffer.

4. (Twice Amended) An information processing system according to claim 1, wherein said memory stores therein said instruction code to be executed on said processor and operand data, and said control circuit prefetches the instruction code and said operand data into said buffer.

5. (Twice Amended) An information processing system according to claim 1, wherein said memory controller further comprising a plurality of buffers, wherein said control circuit transfers data already stored in said plurality of buffers to said processor in an order different from an address order.

---

B23  
12. (Amended) An information processing system according to claim 1, wherein said memory is divided into a first memory for storing therein said instruction code to be executed on said processor and a second memory for

§ 23

storing therein operand data, wherein said access judging circuit for judging whether the memory access from said processor is an access to said first memory or an access to said second memory, said memory controller including a first buffer memory for prefetching of the instruction code and a second memory for prefetching of the operand data; and said control circuit is controlled to prefetch the instruction code into said first buffer memory according to a judgement of said access judging circuit or to prefetch the operand data into said second buffer memory.

---

✓  
Please add new claims 17-29 as follows:

Sub  
B24 DI

--17. An information processing system according to claim 1, wherein said access judging circuit prefetches said instruction code from said memory along said first memory bus and into the buffer.--

--18. An information processing system comprising:

processor;

a memory;

a memory controller;

a system bus connecting said processor and said memory controller;

a first memory bus connecting said memory controller and said memory; and

a second memory bus connecting said memory controller and said memory;

said memory controller comprising:

a buffer;

a control circuit to estimate a most probable address to be accessed next in said memory; and

an access judging circuit to prefetch data stored in said most probable address of the memory to the buffer.--

B24  
--19. An information processing system according to claim 18, wherein said memory controller comprises a direct path for transmitting data directly to said processor from said memory therethrough.--

--20. An information processing system according to claim 19, wherein when the memory access from said processor hits data within said buffer, said control circuit transfers the data to the processor, and when the memory access from said processor fails to hit data within said buffer, said control circuit transfers data within said memory to said processor via said direct path.--

--21. An information processing system according to claim 18, wherein said memory stores instruction code to be executed on said processor therein, and said control circuit prefetches the instruction code from the memory pad along the first memory bus to said buffer.--

--22. An information processing system according to claim 18, wherein said memory stores therein instruction code to be executed on said processor and operand data, and said control circuit prefetches the instruction code from the memory and along the first memory bus to said buffer and said control circuit prefetches the instruction code from the memory and along the second memory bus to said buffer.--

?  
this row it  
19

B24

--23. An information processing system according to claim 18, wherein said memory controller further comprises a plurality of buffers, wherein said control circuit transfers data already stored in said plurality of buffers to said processor in an order different from an address order.--

--24. An information processing system according to claim 18, wherein said memory controller includes an instruction decoder and a branching buffer, and when said instruction decoder detects a branch instruction, said control circuit prefetches an instruction code as a branch destination to said branching buffer and, when an access is made from said processor to the instruction code, said control circuit judges whether or not the instruction code hits data within said buffer and said branching buffer.--

--25. An information processing system according to claim 18, wherein said memory controller includes a register for instructing start or stop of a prefetch to said buffer.--

--26. An information processing system according to claim 18, wherein said control circuit is controlled in an initial state to prefetch data already stored at a pre-specified address into said buffer.--

B24

--27. An information processing system according to claim 18, wherein said processor includes an internal cache, and said control circuit prefetches data having a data size of twice or more a line size of said internal cache into said buffer.--

--28. An information processing system according to claim 18, wherein said memory is divided into a first memory for storing therein said instruction code to be executed on said processor and a second memory for storing therein operand data, wherein said access judging circuit judges whether the memory access from said processor is an access to said first memory or an access to said second memory, said memory controller including a first buffer memory for prefetching of the instruction code and a second memory for prefetching of the operand data, and said control circuit prefetches the instruction code to said first buffer memory according to a judgement of said access judging circuit or prefetches the operand data to said second buffer memory.--

--29. An information processing system according to claim 18, wherein said access judging circuit prefetches said instruction code from said memory along said first memory bus and into the buffer.--

---